Benchmark™ Biometric Sensor System for Hearable Devices

Features

- Chest-Strap quality optical heart rate (HR) measurement, HR zone, HR recovery, resting HR, step rate / count, distance cycling cadence, calories, VO2, activity recognition (running/lifestyle), and at-rest R-R interval (RRi*).

  *Note: Sensor measures P-P interval, which correlates with RRi, see Valencell Heart Rate Variability Review for more information.
- The Benchmark™ sensor plus PerformTek™
- Processor minimizes space impact to the hearable design and provides design flexibility
- Sensor module contains an LED, optical detector with data conversion circuitry, and an accelerometer mounted to an IR-filtering window assembly optimized for sensor system accuracy
- PerformTek™ low-power ARM® Cortex® processor performs sensor data processing and provides a communication interface to the system host processor

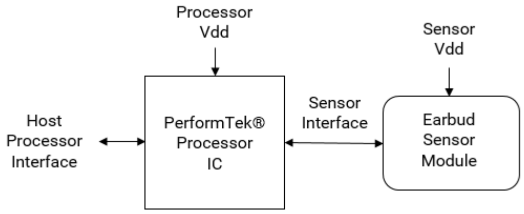
Figure 1: BE2.0 Processor and Sensor with Dime for Scale

- Ear Sensor Dimensions: (10.0 x 4.4 x5.0) mm
- Processor Package: WLCSP-49, 0.4 mm pitch, (3.0 x 3.0 x 0.4) mm
- Sensor Weight 0.175 grams
- 400 kHz I2C or 57.6 kbps UART Interface
- Processor V_{DD}: 1.8 VDC to 3.3 VDC
- Sensor $V_{DD(SENSE)}$: 3.3 VDC
- V_{DD} Current: 1.54 mA standard operating; 5 uA Standby mode; 1 mA in Idle mode
- $V_{DD(SENSE)}$ Current: 0.2 mA standard operating
- Field updatable processor firmware
- Patented optomechanical designs
- 100% factory-tested optical and sensor performance

Description

The PerformTek™ powered Benchmark™ Ear 2.0 Sensor System is the next-generation biometric sensor technology developed by Valencell, Inc. This sensor module supports higher resolution measurements and is almost 30% smaller than our first-generation sensor. This sensor plus the PerformTek™ processor helps you quickly develop your own biometric earbud products. The modular design brings together the best available parts of a successful biometric sensor system in a smaller form factor and includes emitter/detector sensor electronics in an optimized optical package with a processor that is pre-programmed with Valencell's PerformTek™ advanced biometric algorithms.

Figure 2: BE2.0 Simplified Block Diagram



Applications

- In-canal or in-concha wired or wireless headphones
- Hearing aids
- Mono Bluetooth headsets
- Wireless smart audio assistants

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Reference Documentation

Table 1: Related Documents

Document	Title
000638	PerformTek™ Interface Protocol Document
000964	PerformTek™ User Guide
000532	PerformTek™ Earbud Integration Guide
000881	Benchmark™ BE2.0 Sensor Drawing and 3D CAD models
001113	Valencell Heart Rate Variability Review

Change Record

Table 2: Change Record

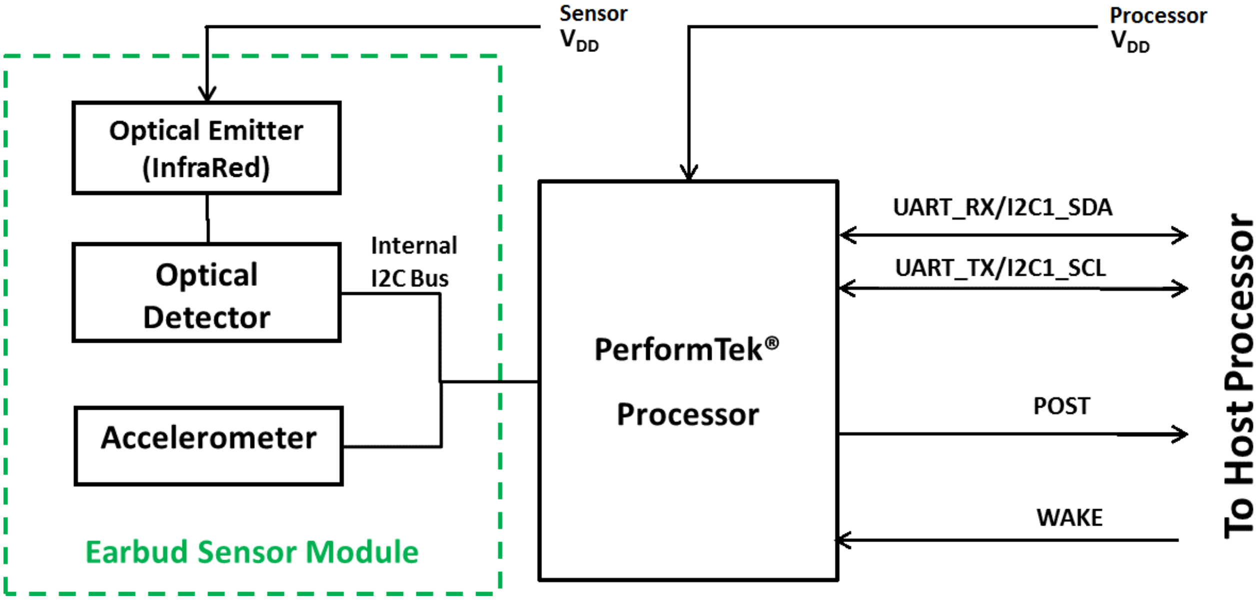
Author	Revision	Date	Description of change(s)
MEP	1.0	06MAR2017	Initial Release
MEP	1.01	15APR2017	- Multiple Formatting changes, and clarified information throughout the document. - Corrected Standby vs Idle Modes - Added information about POST pin's interaction with Bootloader mode. - Updated power consumption numbers based on new firmware release.
MEP	1.02	26MAY2017	- Clarified NRST connection when not driven by Host - Clarified Sensor and MCU current "Conditions" description in Tables 6 and 9. - Performed minor editorial changes

Table of Contents

1 Block Diagram / System Overview

The Benchmark™ Ear 2.0 Biometric Sensor solution is provided in two pieces, the sensor and the PerformTek™ processor. Figure 3 shows how these pieces work together and is described below.

Figure 3: Benchmark™ Ear 2.0 Functional Block Diagram



On the left of the diagram, the sensor module circuit board contains a digital optical detector system, an infrared LED, and an accelerometer. The detector, LED, and accelerometer work together to collect biometric information via reflected light and movement from the wearer. This information is transmitted over the internal I2C bus when requested by the PerformTek™ processor.

The PerformTek™ processor collects the sensor data and runs Valencell's patent protected algorithms to convert the raw measurements into biometric values such as heart rate or cadence and processes those values further into higher level user assessments like calories burned. In addition, sensor module diagnostics such as signal quality, error codes, and serial number ID are available. This information is available to the Host processor via the Host Interface.

The Host Interface is shown on the right side of the diagram. Control lines for interfacing the host processor with the PerformTek™ processor include UART or I2C, Power-On Self-Test (POST), and a Wake-from-Standby line (WAKE).

2 Pin Descriptions

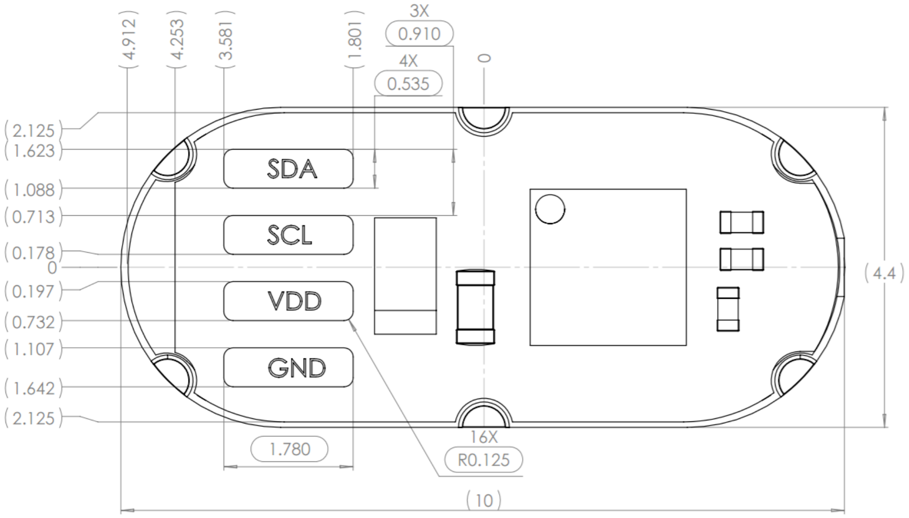
2.1 Sensor Pinout

Table 3 and Figure 4 show the pinout for the Earbud sensor. Solder pads are provided for individual wire or custom flex cable connection.

Table 3: Sensor Pinout

Pin Number	Symbol	Description
1	GND	Connect to system ground / reference plane
2	$V_{DD(SENSE)}$	Sensor 3.3 VDC Power. Connect to sensor supply voltage
3	SCL	I2C Clock Line. Connect to PerformTek™ Processor
4	SDA	I2C Data Line. Connect to PerformTek™ Processor

Figure 4: BE2.0 Sensor Drawing and Solder Pads



2.2 PerformTek™ Processor Pin Description

Table 4 provides a description of the pin assignments to the processor. Pins that are not listed are not connected in the current design implementation. See the STMicroelectronics STM32F401CCY6 device datasheet for processor package information.

Table 4: Processor Pinout

Pin	Name	I/O	Description
A4	SDA	I/O	Sensor I2C data pin. Connect this pin to the sensor I2C bus. A pullup is required on this pin. A series zero ohm resistor should be added to this signal to enable Valencell debug support.
A5	GND	Power	Connect to system ground / reference plane
A6	GND	Power	Connect to system ground / reference plane
A7	V_{DD}	Power	Connect to processor supply voltage
B1	GND	Power	Connect to system ground / reference plane
B2	V_{DD}	Power	Connect to processor supply voltage
B6	PDR_ON	I	Enables processor internal power-on reset. Connect to the processor supply voltage to ensure proper startup of the processor.
B7	VBAT	I	Connect this pin to V_{DD} along with a 0.1uF decoupling capacitor to GND. Do NOT connect to battery voltage.
C4	Host TX/SCL	I/O	Host interface pin configured as either UART TX (processor output) or I2C SCL depending on the selected communication protocol. A pull-up resistor should be added for I2C operation. Connect this pin to the host processor. A series zero ohm resistor should be added to this signal to enable Valencell debug support.
D1	SCL	I/O	Sensor I2C clock pin. Connect this pin to the sensor I2C bus. A pullup is required on this pin. A series zero ohm resistor should be added to this signal to enable Valencell debug support.
D3	GND	Power	Connect to system ground / reference plane

Pin	Name	I/O	Description
D4	RX/SDA	I/O	Host interface pin configured as either UART RX (processor input) or I2C SDA depending on the selected communication protocol. A pull-up resistor should be added for I2C operation. Connect this pin to the host processor. A series zero ohm resistor should be added to this signal to enable Valencell debug support.
D6	OSC OUT	O	Crystal oscillator output. For information on selecting the crystal, refer to the microcontroller specification and the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.
D7	OSC IN	I	Crystal oscillator input
E2	COM Sel	I	Connect to processor supply voltage for I2C Host Interface communication and to system ground for UART communication. Note: For legacy designs that cannot appropriately drive this pin, see the description of the AutoComms feature in Section 4.2.
E6	GND	Power	Connect to system ground / reference plane
E7	NRST	I	Processor reset. A logic low on this pin will reset the processor.
F2	V_{DD}	Power	Connect to processor supply voltage
F6	WAKEUP	I	Wakeup signal from host processor. A low-to-high transition on this pin will wake the processor from Standby Note: The processor will not enter Standby if this signal is not low.

Pin	Name	I/O	Description
G2	VCAP	I	Connect this pin to GND via a 4.7uF capacitor
G4	POST	I/O	This pin serves two functions: 1. Power-On Self Test Output: This pin will present a logic high after the power up process has successfully completed. 2. Bootloader Mode Input: Driving the POST pin high during boot up puts the device into bootloader mode. The POST pin should not be biased during normal operation.

3 Electrical Characteristics

3.1 Sensor

Table 5: Recommended Operating Conditions for Sensor

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sensor Supply Voltage	$V_{DD(SENSE)}$	Min and Max are inclusive of V_{DD} ripple requirement	3.2	3.3	3.6	VDC
Sensor ripple voltage_10	V_{ripple_10}	Sensor system active: 0 to 10 MHz Ripple	-	-	50	mV_{pp}
Sensor ripple voltage_100	V_{ripple_100}	Sensor system active: >10 MHz to 100 MHz Ripple	-	-	100	mV_{pp}
Operating Temperature	-	Device operating in Standby, Idle, or Active Modes	-10	25	50	ºC

Table 6: Operating Characteristics of Sensor

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sensor Current OFF Mode	-	No V_{DD} supply given to sensor module	-	0	-	µA
Sensor Current Standby and Idle Modes	-	System is in Standby mode	-	5	32	µA
Sensor Current Active Mode, Standard-Precision	-	System is in Active mode and operating at standard RRi sampling rate	-	0.204	0.240	mA
Sensor Current Active Mode, High-Precision	-	System is in Active mode and operating at fast RRi sampling rate	-	0.965	1.15	mA
Sensor Current Active Mode, Best-Precision	-	System is in Active mode and operating at fastest RRi sampling rate	-	1.91	2.04	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sensor Pulse Current	I_{pulse}	System is in Active mode	-	23	29	mA

Absolute limits are provided below. If these limits are exceeded, permanent device damage may occur. Additionally, if the sensor is exposed to these limits for an extended period of time, the sensor reliability may be impacted.

Table 7: Sensor Absolute Maximum Limits

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Temperature	-	Device operating in Standby, Idle, or Active Modes – performance not guaranteed	-20	-	70	ºC
Storage Temperature	-	Device powered off, device will require time to come to equalize with normal operating temperature after exposure to limits of storage temperature	-50	-	85	ºC
ESD Rating	-	Human Body Model[1]	-	-	2	kV

Note 1: The sensor module is designed to support system level ESD compliance testing up to 4 kV contact and 8 kV air discharges; however, ESD protection for the standalone sensor module is intended only to protect the sensor during normal handling in a typical electronic manufacturing environment with typical ESD protection in place.

3.2 PerformTek™ Processor

PerformTek™-specific and high-level processor characteristics are provided below. See the processor datasheet for more details.

Table 8: Recommended Operating Conditions for PerformTek™ Processor

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} Supply Voltage[1,2]	V_{DD}	Processor internal Power-On Reset Enabled	1.76	3.3	3.6	V

Note 1: The processor may be operated at 1.80 VDC, with the sensor at 3.3 VDC; however, I2C pullup resistors for the bus between them should be tied to 3.3 VDC to ensure logic level compatibility.

Note 2: V_{DD} must reach or exceed 1.80 VDC on startup to ensure that the internal Processor's Power-On Reset appropriately de-asserts and must stay above 1.76 VDC during operation to avoid Power-Down Reset Assertion. See ST Micro STM32F401x datasheet for more details.

Table 9: Operating Characteristics of PerformTek™ Processor

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I_{DD} Idle Mode	-	System is in Idle mode	-	0.95	-	mA
I_{DD} Standby Mode	I_{STBY}	System is in Standby mode	-	5	-	μA
I_{DD} Active Mode with Standard-Precision RRi[1]	-	System is in Active mode and operating at standard RRi sampling rate	-	1.54 to 1.99	-	mA
I_{DD} Active Mode with High-Precision RRi[1,2]	-	System is in Active mode and operating at fast RRi sampling rate	-	1.90 to 2.35	-	mA
I_{DD} Active Mode with Best-Precision RRi[1,2]	-	System is in Active mode and operating at fastest RRi sampling rate	-	2.45 to 2.90	-	mA
I_{DD} Processor Pulse Current	I_{pulse}	System is in Active mode	-	10	-	mA
Start-up time before POST response	t_{POST}	On Start-up, time measured after V_{DD} equal to or above 1.8V	-	40	150	ms

Note 1: Standard-, High-, and Best-Precision typical ranges depend on if an external oscillator is utilized or not. The external oscillator will further increase precision but will also increase power consumption.

Note 2: High- and Best- precision operation and current draw applies to RRi only. Best-precision heart rate monitoring is available in standard Active Mode.

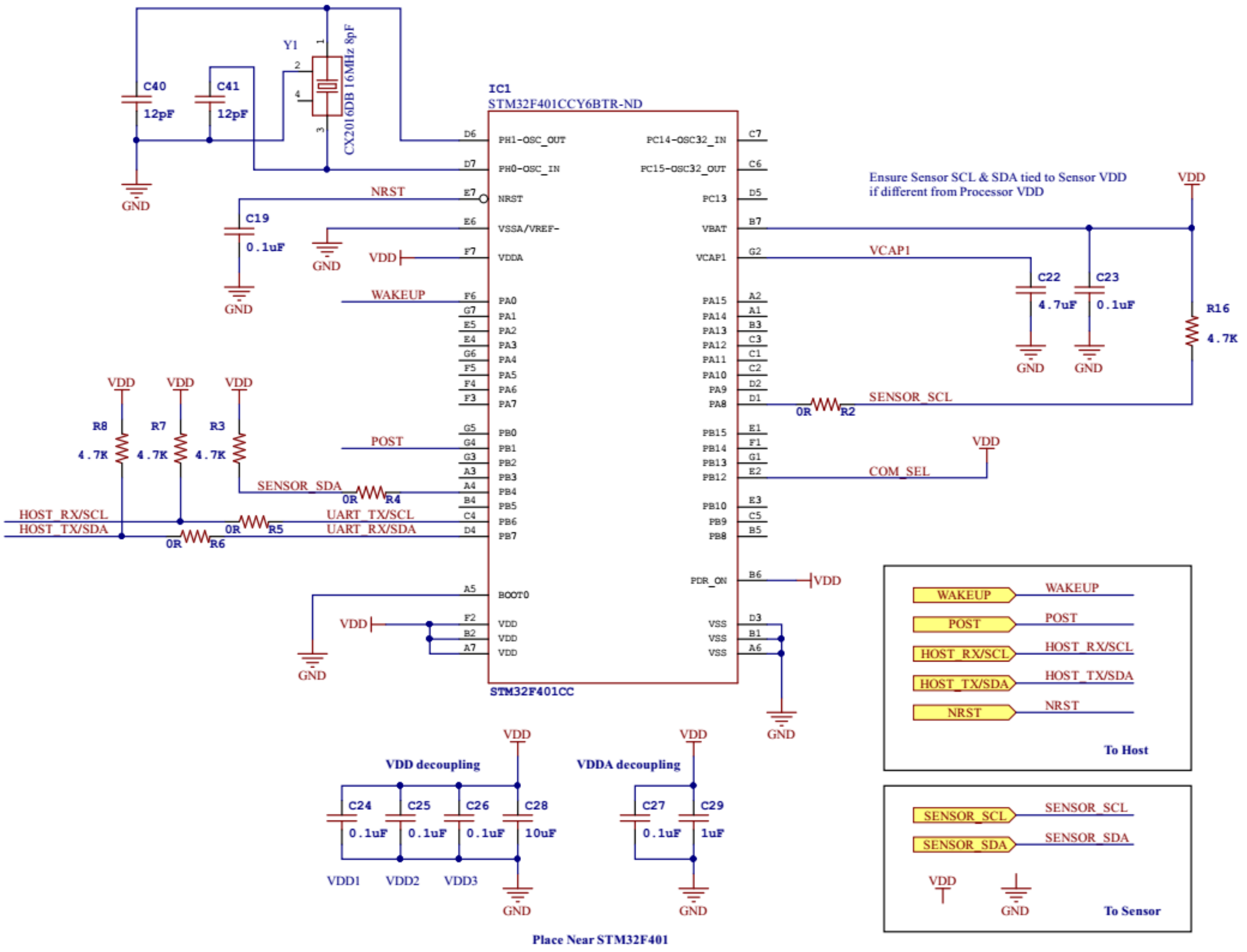
4 PerformTek™ Processor Integration

4.1 PerformTek™ Processor Schematic

The included PerformTek™ Processor is based on the STMicroelectronics STM32F401CCY6.

The processor is programmed by Valencell, Inc. with PerformTek™ custom firmware and algorithms. To interface with this programmed processor, please utilize the schematic diagram and associated interface descriptions that follow. For additional electrical and physical specifications for this processor consult the STM32F401CCY6 datasheet and associated documentation available at www.st.com or contact your local STMicroelectronics sales representative.

Figure 5: Processor Connection Schematic (I2C Host Connection Shown)

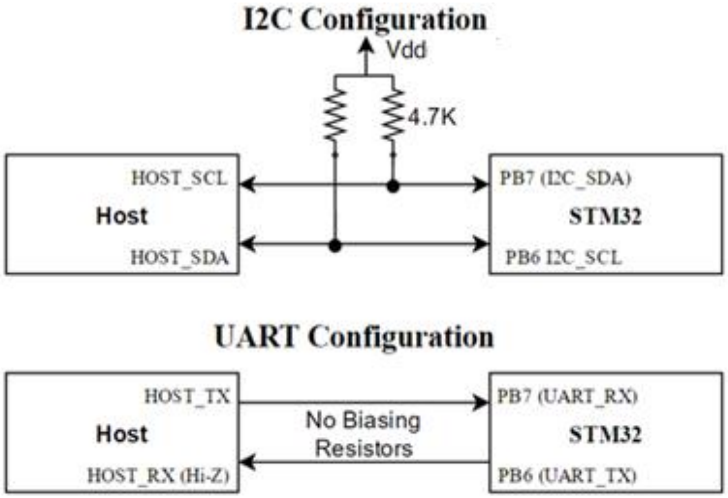


4.2 PerformTek™ Processor Connections

- Host Interface – UART / I2C

The Host Interface that connects the system processor to the PerformTek™ processor supports both I2C and UART communications. This should be selected by tying the COM_SEL pin to Vdd for I2C or Ground for UART communications. While it is recommended that COM_SEL be actively driven to select I2C or UART communications, the processor also provides an automatic communication protocol (AutoComms) selection feature if COM_SEL is not connected. With this feature, the processor monitors its UART_TX pin by applying a weak pull-down to this pin and then reading its status. If the pin is pulled high, it enters I2C communications mode, and if the pin is low, it enters UART communications mode.

Figure 6: AutoComms Compatible Signal Configurations



For proper AutoComms functionality, follow these steps:

1. For a UART interface, no biasing should be added to the communication lines. For I2C, typical pull-up resistor values should be connected between the I2C lines and the Host interface V_{DD}.
2. During PerformTek™ processor bootup, the communication lines should not be driven by the host processor until either the POST pin goes high or t_{POST} as defined in Table 9 has elapsed.

For UART host communications, the UART_RX pin is the receive line for data sent to the module from the host processor and the UART_TX pin is the transmit line from the sensor module to the host. The port settings are 57.6 kbps, 8, N, 1. There is no hardware or software flow control.

For I2C host communications, the I2C _SDA line is the data line and I2C _SCL line is the clock line. The sensor module acts as an I2C slave device with a 400KHz bus speed and an I2C address of 0x44.
For information about the UART or I2C communication protocols, see the PerformTek™ Interface Protocol Document.

- Host Interface – POST (Power-On Self-Test)

  Once V_{DD} power is applied, the PerformTek™ processor will attempt to initialize all components on the module. This startup time is defined by t_{POST} in Table 9. If startup is successful, the POST pin will assert high, otherwise, the pin will stay low. If the POST pin is not utilized, the Max time for t_{POST} should be observed before interaction with the PerformTek™ processor begins.

  Diagnostic information associated with this pin is stored in the sensor module's registers and can be read via the UART/ I2C Host Interface. As part of the POST, the PerformTek processor tests communications with the sensor peripherals and exercises the axes of the accelerometer while checking for a response within bounds. If a failure is detected but the processor can still communicate, the POST will still assert high. To ensure correct system operation, the POST register should be examined at startup. Refer to the PerformTek™ Interface Protocol Document for further information on the POST and other diagnostic registers.

- Host Interface – WAKE

  WAKE is an input to the module used to bring the module out of Standby mode. Raising this pin from Low to High will return the module to an awake state, ready for communication.
  Note that lowering WAKE does not put the module into Standby mode. Low-Power Standby mode is entered via a command over the UART/ I2C module communications. WAKE pin should be lowered before issuing the Standby command. If this pin is not used, it may be tied high to Vdd, but this will prevent the module from entering Standby mode.

- I2C Sensor Interface

  The I2C sensor bus (I2C3) requires pullup resistors to $V_{DD(SENSE)}$. Typical pullup resistor values are shown Figure 5 but may require adjustment depending on your system configuration.

- Crystal Oscillator

  The crystal configuration is used for high accuracy applications and may be omitted for power and space savings when additional inaccuracies from the processor's HSI oscillator can be tolerated. If included, a 16MHz crystal, such as the Kyocera CX2016DB, should be used to maintain software compatibility.

For more information about the processor's HSI accuracy, see the ST Micro STM32F401x datasheet for more details. For information on selecting the crystal, refer to the microcontroller specification and the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

- NRST

  NRST is an active low reset signal connected to the HOST controller to allow it to control reset of the PerformTek™ processor. Valencell recommends connecting this line to the Host controller as part of a robust system reset strategy. However, if this cannot be done, NRST should be tied to a 0.1 µF capacitor placed close to the NRST processor pin as shown in Figure 5.

  Note: Current consumption is undefined while the PerformTek processor is held in reset. NRST should not be used as a method to hold the PerformTek processor in a low power state. Standby mode is the best method for achieving minimum power consumption.

- Decoupling

  The capacitors shown in Figure 5 are necessary to reduce noise and ensure measurement accuracy and proper processor functionality. These capacitors should be placed physically near the VDD pins of the processor.

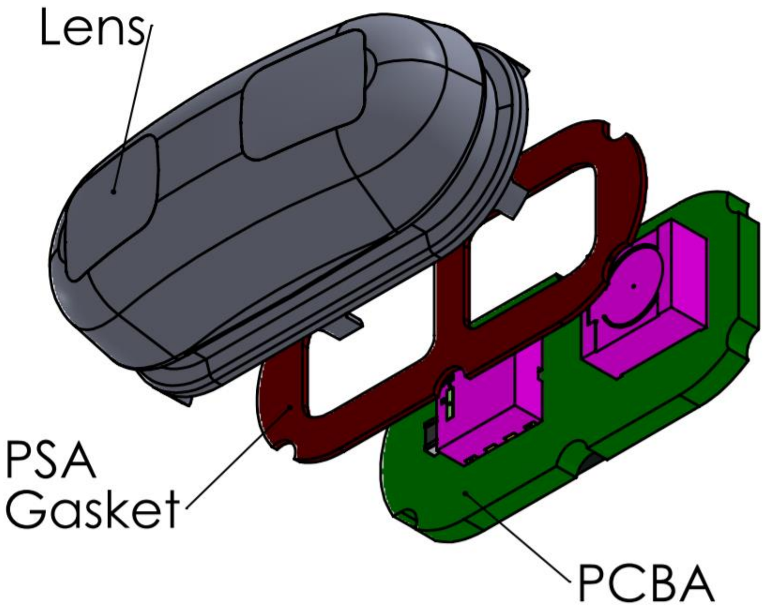
- Firmware Updates

  The PerformTek™ processor supports in-field firmware updates via the Host Interface. Driving the PerformTek™ processor's POST pin high during boot up puts the device into bootloader mode. The POST pin should not be biased during normal operation. Refer to the PerformTek™ User Guide for further information on this feature.

5 Sensor Optical-Mechanical Integration

The sensor component is a critical part of the measurement system and is designed to ensure good optical coupling from the emitter and detector to the user's skin. Placement and proper integration of the sensor into the earbud housing is critical for accurate measurement. The lens frame is a two-shot molded PC opaque frame onto an optical grade PC lens. The PCB and optomechanical lens is tested at module production as an assembly and should not be disassembled.

Figure 7: Earbud Sensor Image



The optical lens system is shown in Figure 7. There is a mating rib along the outer edge of the lens frame. This rib is used as a capture feature to ensure a good seal using adhesive to the customer's earbud enclosure.

The mechanical design has been optimized to reduce the impact of the sensor module on the industrial design, while still maintaining the necessary positioning for sensor accuracy. It is designed for easy integration into the shell of an earbud and the design balance provides optimal sensor accuracy with minimal disruption to other components of the interior of the earbud design.

For capture feature design and adhesive process guidelines and more complete details on sensor integration refer to the Benchmark™ Ear Sensor Integration Guide and BE1.2 Sensor 2D and 3D CAD models.

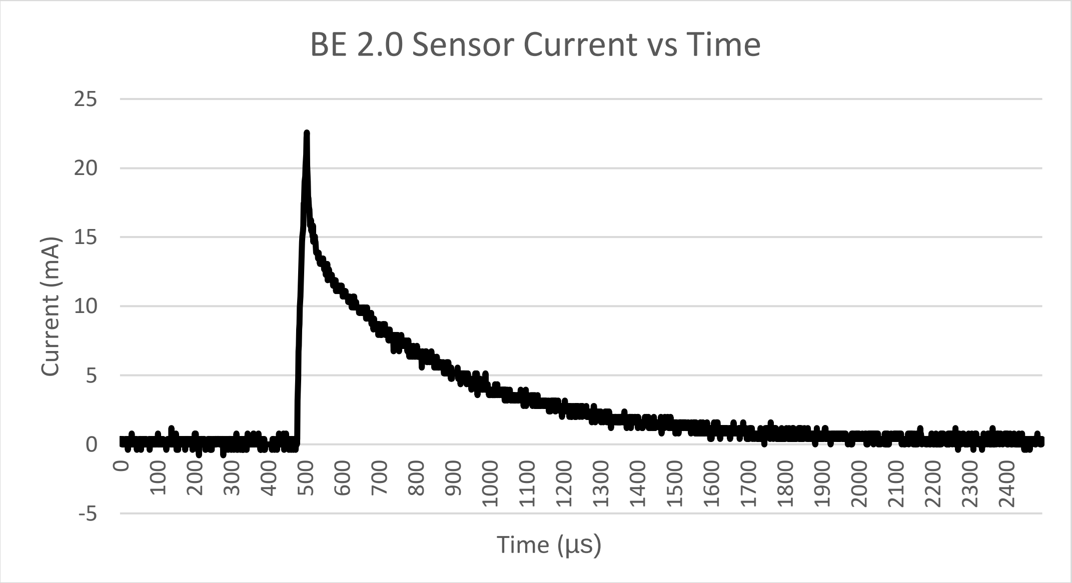
6 Additional Design Guidelines

6.1 Power Supply Design Guidelines

The PerformTek™ processor and sensor may be supplied from the same rail (V_{DD} and $V_{DD(SENSE)}$ combined) or may be supplied separately. If they are supplied together, care must be taken to ensure that the voltage tolerances and ripple specifications for the sensor are still followed. The system power supply or supplies should be designed to meet the requirements in Section 3 during transients from both the Benchmark™ sensor and processor.

Peak $V_{DD(SENSE)}$ current will be periodic where the period of the peaks will depend on the mode of operation Heart Rate and Standard-Precision RRi (40 ms), High-Precision RRi (8 ms), and Best-Precision RRi (4 ms). A typical current peak profile for sensor $V_{DD(SENSE)}$ is shown in Figure 8.

Figure 8: Typical BE2.0 Sensor Current Pulse



The $V_{DD(SENSE)}$ current profile shown here and the V_{DD} current peak listed in Section 3 are based on measured system performance. Processor V_{DD} current peaks are of smaller amplitude and much smaller duration than $V_{DD(SENSE)}$ current peaks. Actual peak and average V_{DD} processor current peak and average numbers will vary depending on the unique characteristics of the system design and how the PerformTek™ features are used within the system. Because of this, Valencell recommends testing our sensors in a manner representative of their intended use as early as possible in the design cycle. To facilitate this, Valencell supplies development kits that support early prototyping and power measurement and can provide design support and review services upon request.

6.2 Audio Quality Design Guidelines

While the Benchmark sensor does not generate any perceptible audible noise on its own, it is possible for system power supply noise or crosstalk from the sensor I2C lines to interfere with audio quality if appropriate system design considerations are not followed. To mitigate potential noise issues, design considerations should include:

- Good power and ground plane design and decoupling to minimize conducted system noise into sensor and / or audio cabling
- Appropriate audio circuit and system grounding to ensure any coupled noise is either returned to the system reference as appropriate or blocked by appropriate isolation
- Isolation of audio circuitry signals from sensor I2C, power, and ground lines to minimize crosstalk (This may be accomplished by a combination of PCB routing and or cable design as appropriate)

7 Processor Communication Interface Example

An example of the processor communications interface protocol is described in short detail below. Simple packet based commands are used to Get or Set measurement readings or parameters, or to control the PerformTek™ processor. For a full description of the interface protocol, please refer to the 000638 Valencell PerformTek™ Interface Protocol document.

- Command: Get(0x08)

The GET command issues requests for parameters and measured values from the PerformTek™ output registers. The purpose of these register values can range from declarations about the firmware features to the most recently calculated value for heart rate.

Following is an example of a GET command that requests three values (heart rate, step rate, and calories):

PerformTek™ Start	Byte Count	GET Command	BPM Request	SPM Request	CALS Request
0x44	0x04	0x08	0x20	0x30	0x42

- Command: Set (0x04)

The SET command writes configuration values to PerformTek™ registers. The purpose of these register values can range from declarations about the capability of the application, to information needed by the algorithms about the user.

Here is an example of a typical SET command that sends three user information parameters (age, gender, and weight):

PerformTek™ Start	Byte Count	SET Command
0x44	0x0A	0x04

. . .

. . .

age	34.5 years old		gender	female		weight	140 lbs	
0x10	0x01	0x9E	0x11	0x00	0x00	0x12	0x02	0x7B

Other interface commands control PerformTek™ processor operation. For full specifications, consult the PerformTek™ Interface Protocol document.

8 Benchmark™ Sensor Ordering Guide

Part Number	Description
000945	Benchmark™ Ear 2.0
000915	Benchmark™ Ear 1.2
001034	Benchmark™ Wrist 2.0
000954	Benchmark™ Wrist 1.2

9 Incoming QC Module Test Fixture

Benchmark™ sensors are 100% optically tested at the factory using a Valencell-designed VIPER test fixture. As an option, these VIPER test fixtures are available for customers to use as part of their incoming inspection process. The test fixtures are available for purchase – please contact Valencell, Inc. for pricing, availability, and additional details.

10 Valencell Product Development Design and Test Services

Valencell has years of experience helping customers bring accurate biometric hearable and wearable devices to market. Much of our experience has been captured in application notes and in the integration and user guides, but additional design and test support is available upon request to help reduce your time to market and lower your technical development risks. Our support can span all stages of the product development process, from concept development through mass production and marketing. Design support examples include assisting with placement and mechanical integration of the sensor module within the product being worn; product fit and comfort; power-supply design; and audio design considerations for hearable designs.

Additionally, product performance should be backed by a solid test plan. Valencell has a sophisticated exercise and sport physiology test lab where products using our sensors are tested for proper performance. Our biometric sensors have been tested on thousands of test subjects with the statistical analysis done in a way that conforms to medical and sports journal publication standards. Testing is carried out both indoors and outdoors under many different activities with pools of subjects that have different skin tones, weight, hair, and fitness levels. Results from our sensor tests can be seen in the form of technical white papers on the Valencell website here: www.valencell.com/white-papers. Valencell Labs is located in the U.S. where there is a good diversity of test subjects. Our lab can validate the accuracy and performance of your product design and provide a statistical analysis as part of a design feedback report along with suggestions to improve the product design. This type of testing is the best and only way to know how well your product will perform when introduced into the market.

For more information about our support options, please contact Valencell.

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